IN THE CLAIMS

All currently pending claims 1-12 and status identifiers are set forth below.

1. (Previously Presented) A system comprising:

a processor;

a power supply coupled to the processor; and

a device coupled to the processor and the power supply and comprising:

> an internal power supply bus configured to receive a power signal from the power
>
> supply; and
>
> an isolation circuit configured to disconnect the internal power supply bus from the
>
> power supply by interrupting the flow of the power signal when a standby
>
> mode is indicated by a control signal received at the isolation circuit.

2.   (Original) The system, as set forth in claim 1, wherein the system is a cellular phone.

3.   (Original) The system, as set forth in claim 1, wherein the system is a personalized digital assistant (PDA).

4.   (Original) The system, as set forth in claim 1, wherein the system is a handheld computer.

5.   (Original) The system, as set forth in claim 1, wherein the device comprises a memory device.

6.   (Original) The system, as set forth in claim 1, wherein the internal power supply bus is configured to provide the power signal to the device.

7.   (Original) The system, as set forth in claim 1, wherein the isolation circuit is coupled between a pad on the device configured to receive the power signal and the internal power supply bus.

8.   (Original) The system, as set forth in claim 1, comprising an input buffer comprising a control line configured to control the isolation circuit.

9.   (Original) The system, as set forth in claim 8, wherein the isolation circuit comprises a p-channel field effect transistor (FET).

10.   (Original) The system, as set forth in claim 9, wherein the gate of the p-channel FET is coupled to the control line of the input buffer.

11.   (Original) The system, as set forth in claim 1, comprising an output buffer configured to buffer the device from the remainder of the system.

12.   (Original) The system, as set forth in claim 11, comprising:

an input/output pad; and

circuitry coupled between the output buffer and the input/output pad and configured to tri-state the input/output pad.

13-36. (Cancelled).